## REMARKS

### *Claim 4*

Applicant has amended claim 4 to recite, in part, "wherein a voltage across a ferroelectric layer of each memory cell equal to the fraction of the programming voltage is sufficient to cause a reversal of polarity of each memory cell." This amendment is not made in response to any rejection on the merits, but because Applicant noticed that the original claim misstated what Applicant intended to claim. Applicant contends that support for the amendment can be found at least in paragraph 0052 of the Specification.

### *Claim Rejections Under 35 U.S.C. § 103*

Claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamura et al. (U.S. Patent No. 6,356,475).

Claim 1 is amended to recite, in part, "placing the selected memory cell in a normally-on state as a result of applying the programming voltage to the first word line and the ground potential to the first program line and the first bit line." Applicant contends that this limitation is supported by at least paragraphs 0043 and 0054 of the Specification. Paragraph 0043 ("Each transistor of each word line 202 can have a first programmed state representing a first data value, such as a data value of 1, or a second programmed state representing a second data value, such as a data value of 0. [. . .] In the first programmed state, the additional positive voltage at the gate dielectric layer 203 will attract electrons, such that the transistor is activated at a zero gate/source voltage corresponding to an 'on' state."); Paragraph 0054 ("In Figure 7A, to write the first data value, the bit line, program line, and word line of all non-selected rows and columns (BL1, PL1, and WL1 in this drawing) are set to some fraction of Vpp in order to avoid disturbing the polarity of the non-selected memory cells. For one embodiment, the bit line, program line, and word line of all non-selected rows and columns are set to approximately Vpp/2 (3V in this example). The selected bit line (BL0) and program line (PL0) are set to a ground potential, i.e., 0V. The selected word line (WL0) is set to Vpp (6V in this example). . . .").

Applicant contends that Tamura et al. expressly teaches that its memory cell is placed in a normally-off state as a result of such programming. Tamura et al., column 87, lines 19-52 ("As a result, the memory cell is set to a normally-off state."). Accordingly, Applicant contends that Tamura et al. expressly teaches away from at least this limitation of claim 1. No secondary reference or reasoned statement was provided that would overcome this failure of the primary reference.

In view of the foregoing, Applicant respectfully submits that claim 1 is patentably distinct from the cited reference. As claims 2-4 depend from and further define patentably distinct claim 1, these claims are also believed to be allowable. Applicant thus respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a), and allowance of claims 1-4.

## *Double Patenting Rejection*

Claims 1-3 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 of co-pending U.S. Patent Application No. 10/339,041. Applicant is submitting herewith a Terminal Disclaimer to overcome this rejection. Applicant thus respectfully requests reconsideration and withdrawal of the rejection, and allowance of claims 1-3.

## CONCLUSION

Claims 1 and 4 are amended herein. Claims 1-4 are now pending.

Applicant believes that all of the pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2204.

Respectfully submitted,

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